Amendments to the Claims:

Claims 1, 9 and 10 are proposed to be amended herein. New claims 21-24 are proposed. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Amended three times) A DRAM circuit comprising:

a substrate having a an active region thereon and capacitor structure disposed ~~thereon~~ above said active region, said capacitor structure including a storage node, a dielectric layer overlying said storage node, and a conductive cell plate overlying said dielectric layer, each of said dielectric layer and said conductive cell plate having an end portion proximate a conductive contact, said conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of said conductive cell plate;

a first TEOS layer disposed proximate said storage node;

a second TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and said conductive cell plate, said second TEOS layer disposed between said capacitor structure and said conductive contact; and

a doped BPSG layer disposed over said second TEOS layer, said conductive contact extending through said BPSG layer and said second TEOS layer.

Claims 2-3 (Canceled)

4. (Original) The DRAM circuit of claim 1, wherein each of said storage node and said conductive cell plate are heavily doped with dopants.

5. (Original) The DRAM circuit of claim 1, wherein each of said storage node and said conductive cell plate comprise a phosphorous-doped polysilicon.

6. (Original) The DRAM circuit of claim 1, wherein said dielectric layer comprises a capacitor cell dielectric layer.

7. (Original) The DRAM circuit of claim 1, wherein said dielectric layer comprises a nitride layer.

8. (Original) The DRAM circuit of claim 1, wherein said capacitor structure comprises a container-shaped capacitor.

9. (Amended three times) The DRAM circuit of claim 1, wherein said second TEOS layer is a dopant barrier between said capacitor structure and said BPSG layer.

10. (Amended four times) A semiconductor memory device comprising:

a semiconductor substrate having an active region thereon and a capacitor structure formed ~~thereon~~ above said active region, said capacitor structure including a first conductive layer, a second conductive layer, and a dielectric layer, said dielectric layer disposed between said first and second conductive layers, each of said dielectric layer and said first and second conductive layers having an end portion proximate a conductive contact, said conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of each of said first conductive layer and said second conductive layer;

a diffusion barrier proximate said first conducting layer and configured to prevent diffusion of contaminants into said active region;

a TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and each of said first conductive layer and said second conductive layer,

said TEOS layer disposed between said capacitor structure and said conductive contact; and

a doped BPSG layer disposed over said TEOS layer, said conductive contact extending through said BPSG layer and said TEOS layer.

Claims 11-12 (Canceled)

13. (Original) The device of claim 10, wherein said conductive contact comprises at least one of metal and conductively doped polysilicon.

14. (Original) The device of claim 10, wherein said conductive contact comprises a digit line.

15. (Original) The device of claim 10, wherein each of said first conductive layer and said second conductive layer are heavily doped with dopants.

16. (Original) The device of claim 10, wherein each of said first conductive layer and said second conductive layer comprise a phosphorous-doped polysilicon.

17. (Original) The device of claim 10, wherein said dielectric layer comprises a capacitor cell dielectric layer.

18. (Original) The device of claim 10, wherein said dielectric layer comprises a nitride layer.

19. (Original) The device of claim 10, wherein said capacitor structure comprises a container-shaped capacitor.

20. (Amended three times) The device of claim 10, wherein said TEOS layer is a dopant barrier between said capacitor structure and said BPSG layer.

Please add the following new claims:

21. (New) The DRAM circuit of claim 1, wherein said first TEOS layer is configured to prevent diffusion of contaminants into said active regions.

22. (New) The DRAM circuit of claim 1, wherein said first TEOS layer comprises a thickness of about 100 Å to about 250 Å.

23. (New) The semiconductor memory device of claim 10, wherein said diffusion barrier comprises a nitride layer or TEOS layer.

24. (New) The semiconductor memory device of claim 10, wherein said diffusion barrier comprises a thickness of about 100 Å to about 250 Å.